SMH Technologies®

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Driver v. 5.07

Moreno Ortolan

Interfacing FlashRunner 2.0 with NORDIC NRF

SMH Technologies S.r.l.

UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

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NORDIC NRF Introduction

Nordic's RF SoCs and SiP

		nRF91 SERIES	nRF53 SERIES	nRF52 SERIES						
		nRF9160	nRF5340	nRF52840	nRF52833	nRF52832	nRF52820	nRF52811	nRF52810	nRF52805
WIRELESS PROTOCOL	LTE-M	●								
	NB-IoT	●								
	GPS	●								
	BLUETOOTH LOW ENERGY		●	●	●	●	●	●	●	●
	BLUETOOTH 5.3		●	●	●	●	●	●	●	●
	LE AUDIO		●							
	DIRECTION FINDING		●		●		●	●		
	2 Mbps		●	●	●	●	●	●	●	●
	LONG RANGE		●	●	●		●	●		
	BLUETOOTH MESH		●	●	●	●	●			
	THREAD		●	●	●		●	●		
	MATTER		●	●						
	ZIGBEE		●	●	●		●			
	ANT		●	●	●	●	●	●	●	●
	2.4 GHz PROPRIETARY		●	●	●	●	●	●	●	●
	NFC		●	●	●	●				
TYPE	SYSTEM-ON-CHIP (SoC)		●	●	●	●	●	●	●	●
	SYSTEM-IN-PACKAGE (SIP)	●								
CORE SYSTEM	CPU	64 MHz Arm Cortex-M33	128 MHz Arm Cortex-M33 + 64 MHz Arm Cortex-M33	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4	64 MHz Arm Cortex-M4
	FPU	●	●	●	●	●				
	DSP INSTRUCTION SET	●	●	●	●	●	●	●	●	●
	CACHE	●	●	●	●	●				
	MEMORY	1 MB Flash, 256 KB RAM	1 MB Flash, 512 KB RAM + 256 KB Flash, 64 KB RAM	1 MB Flash, 256 KB RAM	512 KB Flash, 128 KB RAM	512 KB or 256 KB Flash, 64 KB or 32 KB RAM	256 KB Flash, 32 KB RAM	192 KB Flash, 24 KB RAM	192 KB Flash, 24 KB RAM	192 KB Flash, 24 KB RAM
	CLOCKS	64 MHz / 32 kHz	128 MHz / 64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz	64 MHz / 32 kHz
SECURITY	ARM TRUSTZONE	●	●							
	ARM CRYPTOCELL	310	312	310						
	ROOT-OF-TRUST	●	●	●						
	SECURE KEY STORAGE	●	●							
	AES ENCRYPTION	●	●	●	●	●	●	●	●	●
RADIO	LTE-M/NB-IoT/GPS MODEM	●								
	CERTIFIED LTE BANDS	1-5, 8, 12-14, 17-20, 25-26, 28, 66								
	FREQUENCY	700-2200 MHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
	MAXIMUM TX POWER	23 dBm	3 dBm	8 dBm	8 dBm	4 dBm	8 dBm	4 dBm	4 dBm	4 dBm
	RX SENSITIVITY	-108 dBm (LTE-M), -114 dBm (NB-IoT), -155 dBm (GPS)	-98 dBm (1 Mbps)	-95 dBm (1 Mbps)	-96 dBm (1 Mbps)	-96 dBm (1 Mbps)	-95 dBm (1 Mbps)	-97 dBm (1 Mbps)	-96 dBm (1 Mbps)	-97 dBm (1 Mbps)
	ANTENNA INTERFACE	50 Ω single-ended	Single-ended	Single-ended	Single-ended	Single-ended	Single-ended	Single-ended	Single-ended	Single-ended
PERIPHERALS	HIGH SPEED SPI		●	●	●					
	TWI, SPI, UART	4xTWI/SPI/UART	4xTWI/SPI/UART + TWI/SPI/UART	2xTWI/SPI, SPI, 2xUART	2xTWI/SPI, SPI, 2xUART	2xTWI/SPI, SPI, UART	2xTWI/SPI, UART	TWI/SPI, SPI, UART	TWI, SPI, UART	TWI, SPI, UART
	QSPI		●	●						
	USB		●	●	●		●			
	PWM	4	4	4	4	3		1	1	
	PDM	●	●	●	●	●		●	●	
	I2S	●	●	●	●	●				
	ADC, COMPARATOR	ADC	●	●	●	●	COMP	ADC, COMP	ADC, COMP	ADC
	TIMER, RTC	3,2	3,2 + 3,2	5,3	5,3	5,3	4,2	3,2	3,2	3,2
	TEMPERATURE SENSOR	●	●	●	●	●	●	●	●	●
CERTIFICATIONS		nordicsemi.com/9160cert	CE, FCC	CE, FCC	CE, FCC	CE, FCC	CE, FCC	CE, FCC	CE, FCC	CE, FCC
OPERATING TEMPERATURE		-40 to 85°C	-40 to 105°C	-40 to 85°C	-40 to 105°C	-40 to 85°C	-40 to 105°C	-40 to 85°C	-40 to 85°C	-40 to 85°C
SUPPLY VOLTAGE RANGE		3.0 to 5.5 V	1.7 to 5.5 V	1.7 to 5.5 V	1.7 to 5.5 V	1.7 to 3.6 V	1.7 to 5.5 V	1.7 to 3.6 V	1.7 to 3.6 V	1.7 to 3.6 V
DEVELOPMENT KITS		nRF9160 DK, Nordic Thingy:91	nRF5340 DK, nRF5340 Audio DK	nRF52840 DK, nRF52840 Dongle	nRF52833 DK	nRF52 DK, Nordic Thingy:52	nRF52833 DK	nRF52840 DK	nRF52 DK	nRF52 DK
PACKAGES		10x16x1.04 mm LGA	7x7 mm aQFN94 (48 GPIOs), 4.4x4.0 mm WLCSP95 (48 GPIOs)	7x7 mm aQFN73 (48 GPIOs), 6x6 mm QFN48 (30 GPIOs), 3.5x3.6 mm WLCSP94 (48 GPIOs)	7x7 mm aQFN73 (42 GPIOs), 5x5 mm QFN40 (18 GPIOs), 3.2x3.2 mm WLCSP (42 GPIOs)	6x6 mm QFN48 (32 GPIOs), 3.0x3.2 mm WLCSP50 (32 GPIOs)	5x5 mm QFN40 (18 GPIOs), 2.53x2.53 mm WLCSP44 (18 GPIOs)	6x6 mm QFN48 (32 GPIOs), 5x5 mm QFN32 (17 GPIOs), 2.48x2.46 mm WLCSP33 (15 GPIOs)	6x6 mm QFN48 (32 GPIOs), 5x5 mm QFN32 (17 GPIOs), 2.48x2.46 mm WLCSP33 (15 GPIOs)	2.48x2.46 mm WLCSP28 (10 GPIOs)

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nRF54L15

Description: The nRF54L15 is an ultra low power multiprotocol SoC for Bluetooth LE, Bluetooth Mesh, Thread, Matter, ANT+ and 2.4 GHz proprietary protocols with a new 4 Mbps throughput option. The nRF54L Series enhances the popular nRF52 Series with greater processing power and efficiency, more memory, security and new peripherals – all in a more compact package.

Technical details: nRF54L15 doubles the processing power of nRF52840 SoC while reducing power consumption. This processing efficiency, combined with a low power consumption radio and low sleep currents, extends battery life or allows for a reduction in form factor by using smaller batteries. Larger memory enables multiple RF protocols to run concurrently and aids firmware update functionality. The radio brings lower latency and longer range with up to 8 dBm TX power and -98 dBm RX sensitivity for 1 Mbps Bluetooth LE. The nRF54L15 offers security services such as Secure Boot, Secure Firmware Update and Secure Storage. It is designed for PSA Certified Level 3.

Tech Spec

Processing
128 MHz Arm Cortex-M33 processor

Memory
1.5 MB non-volatile memory, 256 KB RAM

New peripherals
Global RTC, 14-bit ADC, Software-defined peripheral enabled by a RISC-V coprocessor

Security
Designed for PSA Certified Level 3 IoT security standard

nRF54H20

Description: The nRF54H20 is a revolutionary multiprocessor and multiprotocol SoC for Bluetooth LE (supporting all Bluetooth 5.4 features), LE Audio, Bluetooth Mesh, Thread, Matter, ANT+ and 2.4 GHz proprietary protocols with a new 4 Mbps throughput option.

Technical details: The nRF54H20 features multiple processors optimized for specific types of workloads. The application processor was tested with ULPMark-CoreMark and outclassed other wireless SoCs and low-power general purpose MCUs both in processing performance and efficiency. The nRF54H20's radio offers long range and improved robustness with 10 dBm TX power, 100 dBm RX sensitivity for Bluetooth LE and -104 dBm for 802.15.4. In addition to remarkable processing power, ample memory and best-in-class radio, the SoC is also equipped with advanced peripherals and state-of-the-art security features, including physical protection. The nRF54H20 will enable developers to build revolutionary IoT products, with simpler designs, reduced sizes, longer battery life and the ability to perform more advanced tasks, including the execution of machine learning models.

Tech Spec

Processing
Multiple Arm Cortex-M33 processors (clocked up to 320 MHz), Multiple RISC-V coprocessors

Memory
2 MB non-volatile memory, 1 MB RAM

Advanced peripherals
High-speed USB (480 Mbps), CAN FD controller, 2x I3C, 14-bit ADC

Security (in bold)
Designed for PSA Certified Level 3 IoT security standard

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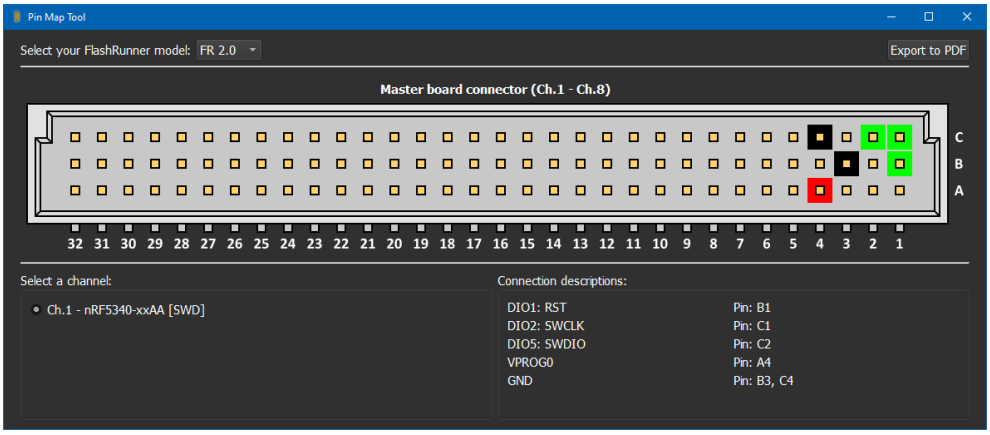
NORDIC NRF Protocol and PIN map

NRF devices support the SWD protocol.

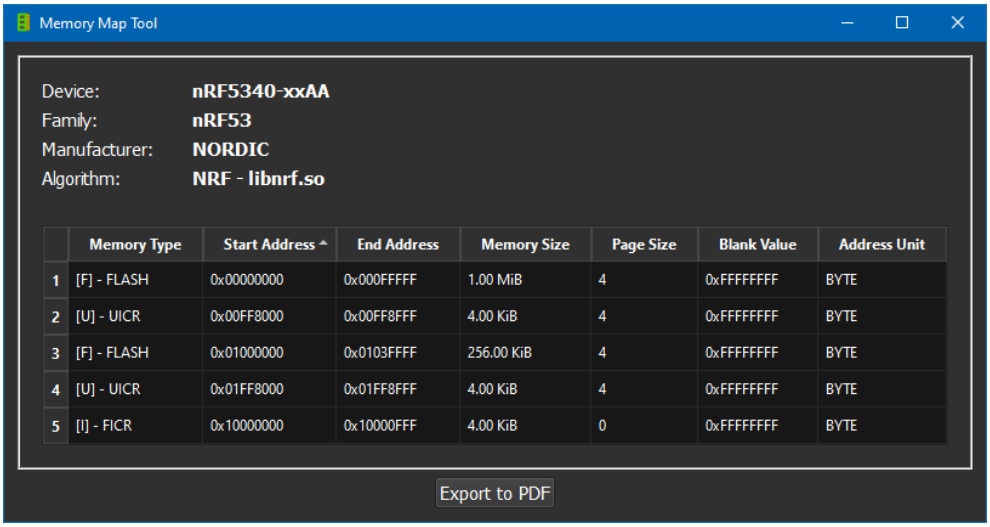
```
#TCSETPAR CMODE <SWD>
```

NORDIC NRF PIN MAP



NORDIC NRF Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - FLASH	0x00000000	0x000FFFFF	1.00 MiB	4	0xFF	BYTE
[U] - UICR	0x00FF8000	0x00FF8FFF	4.00 KiB	4	0xFF	BYTE
[F] - FLASH	0x01000000	0x0103FFFF	256.00 KiB	4	0xFF	BYTE
[U] - UICR	0x01FF8000	0x01FF8FFF	4.00 KiB	4	0xFF	BYTE
[I] - FICR	0x10000000	0x10000FFF	4.00 KiB	0	0xFF	BYTE



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NORDIC NRF Access Port Protection

Access port protection blocks the debugger from read and write access to all CPU registers and memory mapped addresses when enabled.

Access port protection is enabled and disabled differently depending on the build code of the device.

NORDIC NRF Access Port Protection for Device Revision <= Xxx

This information refers to build codes Xxx and earlier.

nRF52 series

- nRF52840: Xxx = **D**
- nRF52833: Xxx = **A**
- nRF52832: Xxx = **F**
- nRF52820: Xxx = **C**
- nRF52811: Xxx = **A**
- nRF52810: Xxx = **D**
- nRF52805: Xxx = **A**

By default, access port protection is disabled.

Access port protection is enabled by writing UICR.APPROTECT to Enabled and performing any reset.
Access port protection is disabled by issuing an ERASEALL command via CTRL-AP.
This command will erase the flash, UICR, and RAM, including UICR.APPROTECT.
Erasing UICR will set UICR.APPROTECT value to Disabled.

NORDIC NRF Access Port Protection for Device Revision >= Xxx

This information refers to build codes Xxx and later.

nRF52 series

- nRF52840: Xxx = **F**
- nRF52833: Xxx = **B**
- nRF52832: Xxx = **G**
- nRF52820: Xxx = **D**
- nRF52811: Xxx = **B**
- nRF52810: Xxx = **E**
- nRF52805: Xxx = **B**

By default, access port protection is enabled.

Access port protection is disabled by issuing an ERASEALL command via CTRL-AP.
Read CTRL-AP APPROTECTSTATUS to ensure that access port protection is disabled, and repeat the ERASEALL command if needed.
This command will erase the flash, UICR, and RAM.

Access port protection will remain disabled until one of the following occurs:

- Pin reset
- Power or brownout reset
- Watchdog reset if not in Debug Interface Mode, see Debug Interface mode on page 56
- Wake from System OFF if not in Emulated System OFF

To keep access port protection disabled, the following actions must be performed:

- Program UICR.APPROTECT to Hw Disabled.
  This disables the hardware part of the access port protection scheme after the first reset of any type.
  The hardware part of the access port protection will stay disabled as long as UICR.APPROTECT is not overwritten.
- Firmware must write APPROTECT.DISABLE to Sw Disable. This disables the software part of the access port protection scheme.

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Note: *Register APPROTECT.DISABLE is reset after pin reset, power or brownout reset, watchdog reset, or wake from System OFF as mentioned above.*

The following figure is an example on how a device with access port protection enabled can be erased, programmed, and configured to allow debugging.

Operations sent from debugger as well as registers written by firmware will affect the access port state.

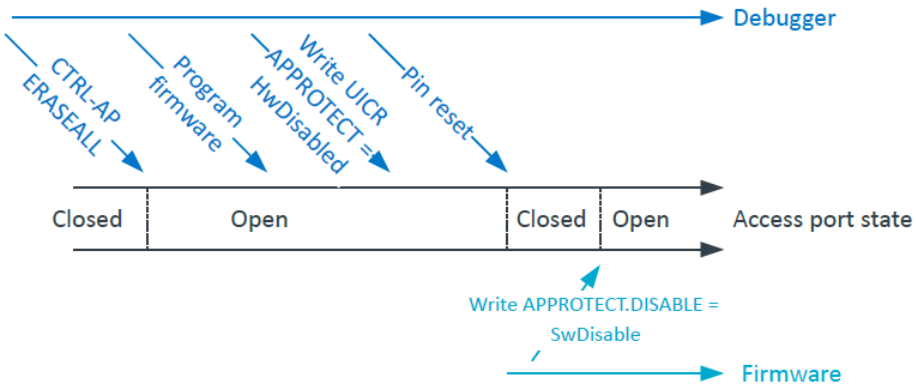

Figure 8: Access port unlocking

Access port protection is enabled when the disabling conditions are not present.
For additional security, it is recommended to write Enabled to UICR.APPROTECT, and have firmware write Force to APPROTECT.FORCEPROTECT.

This is illustrated in the following figure.

Note: *Register APPROTECT.FORCEPROTECT is reset after any reset.*

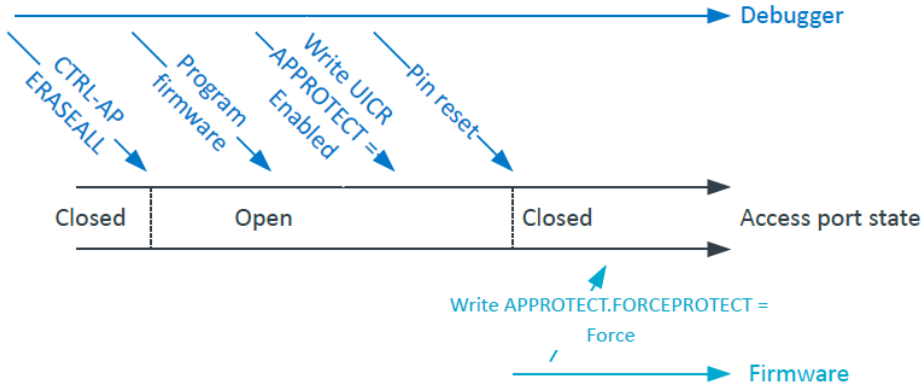

Figure 9: Force access port protection

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NORDIC NRF Driver Parameters

The standard parameters are used to configure some specific options inside NRF driver.

#TCSETPAR ENTRY_CLOCK

Syntax: `#TCSETPAR ENTRY_CLOCK <Frequency>`

<Frequency> Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the JTAG/SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR SAMPLING_POINT

Syntax: `#TCSETPAR SAMPLING_POINT <Value>`

<Value> Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

Note: Default value 17

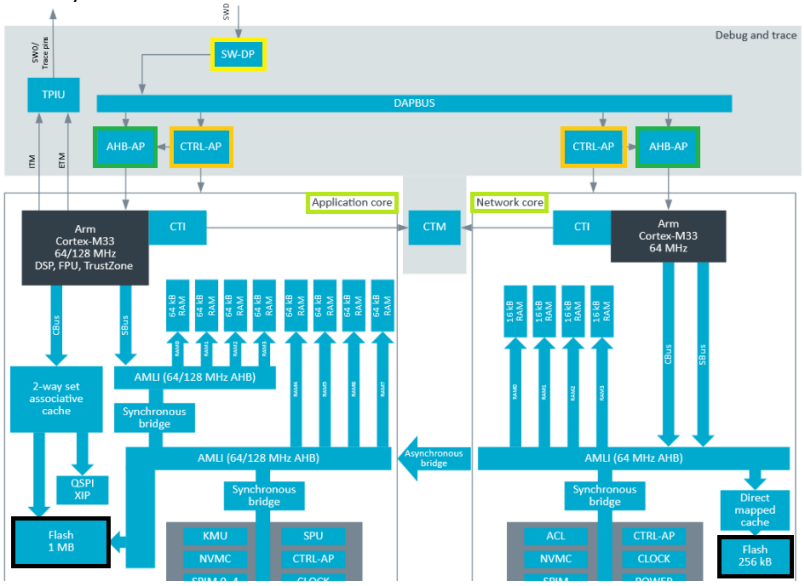
#TCSETPAR SELECT_CORE

Syntax: `#TCSETPAR SELECT_CORE <Core>`

<Core> Accepted values are: BOTH_CORES, APPLICATION_CORE and NETWORK_CORE

Description: Use this parameter to select the **nRF5340** core
If you select BOTH_CORES you can program Flash and UICR memories of both cores in the same moment
If you select APPLICATION_CORE or NETWORK_CORE you can program Flash and UICR memory of selected core

Note: Default value BOTH_CORES
Available only for **nRF5340** device



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NORDIC NRF Driver Commands

Here you can find the complete list of all available commands for NRF driver.

```
Memory type:

C → Chip (Only for Masserase command)
F → FLASH
U → UICR
I → FICR
```

```
Core abbreviations:

APP → Application Core (only for NRF5340 device)
NET → Network Core (only for NRF5340 device)
```

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

Example for nRF52 series:

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 1.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 1.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
AP[1] IDR: 0x02880000, Type: JTAG connection.
The device access port protection is disabled.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x410FC241.
Implementer Code: 0x41-[ARM].
Found Cortex M4 revision r0p1.
Cortex M4 core Halted [0.002 s].
Single core device configuration:
 * Code Page Size: 0x00001000, Code Size: 0x00000100.
 * Total Code Space 0x00100000.
 * Device ID: 0x1A3B0CA8D89202EE.
 * Part: 0x52840 - nRF52840.
 * Variant: 0x41414630 - AAF0 - Revision F.
 * Package: 0x2004 - QIxx - 73-pin aQFN.
 * Ram Size: 0x100 - 256 kByte RAM.
 * Flash Size: 0x400 - 1024 kByte FLASH.
Requested Clock is 1.00 MHz.
Generated Clock is 1.00 MHz.
Good samples: 16 [Range 0-15].
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 1.00 MHz.
Internal Watchdog Disabled.
Time for Connect: 0.115 s.
>|
```

Example for nRF53 series:

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
```


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```
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[2] IDR: 0x12880000, Type: JTAG connection.
AP[3] IDR: 0x12880000, Type: JTAG connection.
Application core protections:
 * Access Port Protection is disabled.
 * Secure Protection is disabled.
Network core protections:
 * Access Port Protection is disabled.
 * Secure Protection is disabled.
Cortex M33 Application core:
 * AP[0] ROM table base address 0xE00FF000.
 * AP[0] CPUID: 0x410FD214.
 * AP[0] Implementer Code: 0x41 - [ARM].
 * AP[0] Found Cortex M33 revision r0p4.
 * AP[0] Cortex M33 core halted [0.001 s].
Cortex M33 Network core:
 * AP[1] ROM table base address 0xE00FF000.
 * AP[1] CPUID: 0x410FD214.
 * AP[1] Implementer Code: 0x41 - [ARM].
 * AP[1] Found Cortex M33 revision r0p4.
 * AP[1] Cortex M33 core halted [0.001 s].
Application core:
 * AP[0] Code: Page 0x1000, Size: 0x0100.
 * AP[0] Total Code Space 0x00100000.
 * AP[0] Device ID: 0x7AC4600A30170BBB.
 * AP[0] Part: 0x5340 - nRF5340.
 * AP[0] Variant: 0x41414141 - AAAA.
 * AP[0] Package: 0x2000 - QFxx - 94pin QFN.
 * AP[0] Ram Size: 0x200 - 512 kByte RAM.
 * AP[0] Flash Size: 0x400 - 1024 kByte.
Network core:
 * AP[1] Code: Page 0x0800, Size: 0x0080.
 * AP[1] Total Code Space 0x00040000.
 * AP[1] Device ID: 0xFFFFFFFFFFFFFFFF.
 * AP[1] Part: 0x5340 - nRF5340.
 * AP[1] Variant: 0x41414141 - AAAA.
 * AP[1] Package: 0x2000 - QFxx - 94pin QFN.
 * AP[1] Ram Size: 0x040 - 64 kByte RAM.
 * AP[1] Flash Size: 0x100 - 256 kByte.
Requested Clock is 20.00 MHz.
Generated Clock is 20.00 MHz.
Good samples: 1 [Range 7-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 20.00 MHz.
Time for Connect: 0.106 s.
>|
```

#TPCMD MASSERASE

#TPCMD MASSERASE <C|F|U>
C: Masserase command for the entire memory of target device.
F: Masserase command only for Flash memory of target device.
U: Masserase command only for UICR memory of target device.

If this command is executed after the UNPROTECT command, it will be skipped and the message "Masserase already done into Unprotect Procedure" will be printed on the Real Time Log.

For the NRF5340 device if **#TCSETPAR** SELECT_CORE <APPLICATION_CORE / NETWORK_CORE> is added before Masserase command, the MASSERASE command will be executed only on the selected core.
If no core is specified, the MASSERASE command is executed in parallel on both cores of NRF5340 device.

#TPCMD PAGEERASE

#TPCMD PAGEERASE <F> <start address> <size>
This function performs a page erase of Flash memory based on Start Address and Size.
Enter the Start Address and Size in hexadecimal format.

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#TPCMD BLANKCHECK

#TPCMD BLANKCHECK <F|U>
Blankcheck is available for Flash and UICR memory.
Verify if all memory is erased.

#TPCMD BLANKCHECK <F|U> <start address> <size>
Blankcheck is available for Flash and UICR memory.
Verify if selected part of memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <F|U>
Program is available for Flash and UICR memory.
Programs all memory of the selected type based on the data in the FRB file.

#TPCMD PROGRAM <F|U> <start address> <size>
Program is available for Flash and UICR memory.
Programs selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

#TPCMD VERIFY <F|U> <R>
R: Readout Mode.
Verify Readout is only available for Flash and UICR memory.
Verify all memory of the selected type based on the data in the FRB file.

#TPCMD VERIFY <F|U> <R> <start address> <size>
R: Readout Mode.
Verify Readout is available for Flash and UICR memory.
Verify selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY <F|U> <S>
S: Checksum 32 Bit Mode.
Verify Checksum is only available for Flash and UICR memory.
Verify all memory of the selected type based on the data in the FRB file.

#TPCMD VERIFY <F|U> <S> <start address> <size>
S: Checksum 32 Bit Mode.
Verify Checksum is only available for Flash and UICR memory.
Verify selected part of memory based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

#TPCMD READ <F|U>
Read is available for Flash and UICR memory.
Read all memory of selected type.
The result of the read command will be visible into the Terminal.

#TPCMD READ <F|U> <start address> <size>
Read is available for Flash and UICR memory.
Read selected part of memory of the selected type.
The result of the read command will be visible into the Terminal.

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#TPCMD DUMP

`#TPCMD DUMP <F|U>`
Dump is available for Flash and UICR memory.
Dump all memory of selected type.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

`#TPCMD DUMP <F|U> <start address> <size>`
Dump is available for Flash and UICR memory.
Dump selected part of memory of the selected type.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

#TPCMD PROTECT

Syntax: `#TPCMD PROTECT`

Prerequisites: none

Description: Protect target Nordic device.
Enable the Access Port protection.
After the protect command it is no longer possible to execute any commands other than the `#TPCMD UNPROTECT` command.
This command is present in the Nordic devices of the NRF52xx, NRF53xx and nRF91xx series, however it isn't present in the NRF51xx series.

Examples: Correct command execution for ***nRF52*** series: 😊

```
---#TPCMD PROTECT
Try to set access port protection...
Perform a software reset.
Access port protection is not enabled...
Perform a reset using watchdog trigger.
> The device access port protection is enabled.
Time for Protect: 0.067 s.
```

Correct command execution for ***nRF52*** series: 😊

```
---#TPCMD PROTECT
> Device is protected, skipped procedure.
Time for Protect: 0.001 s.
```

Correct command execution for ***nRF53*** series: 😊

```
---#TPCMD PROTECT
Try to set Application core access port protection...
Try to set Network core access port protection...
> The core protection is enabled for both Application and Network cores.
Time for Protect: 0.031 s
```

Correct command execution for ***nRF53*** series: 😊

```
---#TPCMD PROTECT
> Application core is protected, skipped procedure.
> Network core is protected, skipped procedure.
Time for Protect: 0.001 s
```

#TPCMD UNPROTECT

Syntax: `#TPCMD UNPROTECT`

Prerequisites: none

Description: Unprotect target Nordic device.

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Removes the protection on the Access Port enabled by the PROTECT command or by writing the APPROTECT register with a value other than 0xFF.

When the UNPROTECT command is executed the device is erased (both the Flash memory and the UICR memory, while the FICR memory is not erased).

If after an UNPROTECT command the MASSERASE <C|F|U> or PAGEERASE <F|U> command is executed, these are ignored as the device is already in the erased state.

This command is present in the Nordic devices of the NRF52xx, NRF53xx and nRF91xx series, however it isn't present in the NRF51xx series.

Examples: Correct command execution for ***nRF52*** series: 😊

```
---#TPCMD UNPROTECT
Try to remove access port protection...
Perform a software reset.
> The access port protection is removed.
Time for UnProtect: 0.196 s.
```

Correct command execution for ***nRF52*** series: 😊

```
---#TPCMD UNPROTECT
> Device is not protected, skipped procedure.
Time for UnProtect: 0.001 s
```

Correct command execution for ***nRF53*** series: 😊

```
---#TPCMD UNPROTECT
Try to remove Application core access port protection...
Try to remove Network core access port protection...
> The core protection is removed for both Application and Network cores.
Time for UnProtect: 0.031 s
```

Correct command execution for ***nRF53*** series: 😊

```
---#TPCMD UNPROTECT
> Application core is unprotected, skipped procedure.
> Network core is unprotected, skipped procedure.
Time for UnProtect: 0.001 s
```

#TPCMD RUN

Syntax: `#TPCMD RUN <Time [s]>`

<Time [s]>	Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
`#TPCMD RUN <Time [s]>` instead moves the Reset line down and high, waits for the entered time.
This command typically can be used to execute the firmware programmed in the device.

#TPCMD READ_MEM8

Syntax: `#TPCMD READ_MEM8 <Address> <Byte Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<Byte Count>	Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

Description: Read memory byte per byte from target NRF device

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Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target NRF device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target NRF device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function and put the device back in Normal mode to prevent power consumption. Power off and exit.

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NORDIC NRF Driver Examples

Here you can see a complete example of NORDIC NRF projects.

1 – NORDIC nRF52832 example 512KB Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 512KB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD UNPROTECT
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD PROTECT
#TPCMD DISCONNECT
#TPEND
```

1 – NORDIC nRF52832 example 512KB Real Time Log

```
>|
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
AP[1] IDR: 0x02880000, Type: JTAG connection.
The device access port protection is disabled.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x410FC241.
Implementer Code: 0x41-[ARM].
Found Cortex M4 revision r0p1.
Program counter value is 0xFFFFFFFE.
Cortex M4 core Halted [0.001 s].
Single core device configuration:
 * Code Page Size: 0x00001000, Code Size: 0x00000080.
 * Total Code Space 0x00080000.
 * Device ID: 0x6230358074CB9FAB.
 * Part: 0x52832 - nRF52832.
 * Variant: 0x41414230 - AAB0 - Revision B.
 * Package: 0x2000 - QFxx - 48-pin QFN.
 * Ram Size: 0x40 - 64 kByte RAM.
 * Flash Size: 0x200 - 512 kByte FLASH.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 1 [Range 6-6].
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 37.50 MHz.
Internal Watchdog Disabled.
Time for Connect: 0.107 s.
>|
---#TPCMD UNPROTECT
> Device is not protected, skipped procedure.
Time for UnProtect: 0.001 s.
>|
---#TPCMD MASSERASE C
```


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```
Chip Erased: Erased Flash and UICR Memory.
Time for Masserase C: 0.010 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.036 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 8.895 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.227 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.098 s.
>|
---#TPCMD PROTECT
Try to set access port protection...
Perform a software reset.
> The device access port protection is enabled.
Time for Protect: 0.022 s.
>|
---#TPCMD DISCONNECT
>|
```

1 – NORDIC nRF52832 example 512KB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.107 s
Unprotect	0.001 s
Masserase Flash	0.010 s
Blankcheck Flash	0.036 s
Program Flash	8.895 s
Verify Readout Flash	0.227 s
Verify Checksum Flash	0.098 s
Protect	0.022 s
Cycle Time	**00:09.461 s**

2 – NORDIC nRF52840 example 1MB Commands

```
##TCSETPAR ENTRY_CLOCK 1000000
#TCSETPAR PROTCLK 15000000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV PUSHPULL
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 1800
#TCSETPAR CMODE SWD
#TPSETSRC 1MB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD UNPROTECT
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD PROTECT
#TPCMD DISCONNECT
#TPEND
```

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2 – NORDIC nRF52840 example 1MB Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 1.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 1.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x23000000, Type: JTAG connection.
AP[1] IDR: 0x02880000, Type: JTAG connection.
The device access port protection is enabled.
Requested Clock is 15.00 MHz.
Generated Clock is 15.00 MHz.
Good samples: 4 [Range 9-12].
IDCODE: 0x2BA01477.
Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
ID-Code read correctly at 15.00 MHz.
Time for Connect: 0.105 s.
>|
---#TPCMD UNPROTECT
Try to remove access port protection...
Perform a software reset.
> The access port protection is removed.
Time for UnProtect: 0.191 s.
>|
---#TPCMD MASSERASE C
Erase already done into Unprotect procedure.
Time for Masserase C: 0.001 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.064 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 2.375 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 1.136 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.196 s.
>|
---#TPCMD PROTECT
Try to set access port protection...
Perform a software reset.
Access port protection is not enabled...
Perform a reset using watchdog trigger.
> The device access port protection is enabled.
Time for Protect: 0.035 s.
>|
---#TPCMD DISCONNECT
>|
```

2 – NORDIC nRF52840 example 1MB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.105 s
Unprotect	0.191 s
Masserase Flash	0.001 s
Blankcheck Flash	0.064 s
Program Flash	2.375 s
Verify Readout Flash	1.136 s
Verify Checksum Flash	0.196 s
Protect	0.035 s
Cycle Time	**00:04.153 s**

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3 – NORDIC nRF5340 example 1MB + 256KB Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 20000000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC nRF5340-xxAA.frb
#TPSTART
#TPCMD CONNECT
#TPCMD PROTECT
#TPCMD PROTECT
#TPCMD UNPROTECT
#TPCMD UNPROTECT
#TCSETPAR SELECT_CORE BOTH_CORES
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TCSETPAR SELECT_CORE APPLICATION_CORE
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TCSETPAR SELECT_CORE NETWORK_CORE
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPEND
```

3 – NORDIC nRF5340 example 1MB + 256KB Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[2] IDR: 0x12880000, Type: JTAG connection.
AP[3] IDR: 0x12880000, Type: JTAG connection.
Application core protections:
 * Access Port Protection is disabled.
 * Secure Protection is disabled.
Network core protections:
 * Access Port Protection is disabled.
 * Secure Protection is disabled.
Cortex M33 Application core:
 * AP[0] ROM table base address 0xE00FF000.
 * AP[0] CPUID: 0x410FD214.
 * AP[0] Implementer Code: 0x41 - [ARM].
 * AP[0] Found Cortex M33 revision r0p4.
 * AP[0] Cortex M33 core halted [0.001 s].
Cortex M33 Network core:
 * AP[1] ROM table base address 0xE00FF000.
 * AP[1] CPUID: 0x410FD214.
 * AP[1] Implementer Code: 0x41 - [ARM].
 * AP[1] Found Cortex M33 revision r0p4.
 * AP[1] Cortex M33 core halted [0.001 s].
Application core:
 * AP[0] Code: Page 0x1000, Size: 0x0100.
```


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```
 * AP[0] Total Code Space 0x00100000.
 * AP[0] Device ID: 0x7AC4600A30170BBB.
 * AP[0] Part: 0x5340 - nRF5340.
 * AP[0] Variant: 0x41414141 - AAAA.
 * AP[0] Package: 0x2000 - QFxx - 94pin QFN.
 * AP[0] Ram Size: 0x200 - 512 kByte RAM.
 * AP[0] Flash Size: 0x400 - 1024 kByte.
Network core:
 * AP[1] Code: Page 0x0800, Size: 0x0080.
 * AP[1] Total Code Space 0x00040000.
 * AP[1] Device ID: 0xFFFFFFFFFFFFFFFF.
 * AP[1] Part: 0x5340 - nRF5340.
 * AP[1] Variant: 0x41414141 - AAAA.
 * AP[1] Package: 0x2000 - QFxx - 94pin QFN.
 * AP[1] Ram Size: 0x040 - 64 kByte RAM.
 * AP[1] Flash Size: 0x100 - 256 kByte.
Requested Clock is 20.00 MHz.
Generated Clock is 20.00 MHz.
Good samples: 1 [Range 7-7].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 20.00 MHz.
Time for Connect: 0.109 s.
>|
---#TPCMD PROTECT
Try to set Application core access port protection...
Try to set Network core access port protection...
> The core protection is enabled for both Application and Network cores.
Time for Protect: 0.027 s.
>|
---#TPCMD PROTECT
> Application core is protected, skipped procedure.
> Network core is protected, skipped procedure.
Time for Protect: 0.001 s.
>|
---#TPCMD UNPROTECT
Try to remove Application core access port protection...
Try to remove Network core access port protection...
> The core protection is disabled for both Application and Network cores.
Time for UnProtect: 0.560 s.
>|
---#TPCMD UNPROTECT
> Application core is not protected, skipped procedure.
> Network core is not protected, skipped procedure.
Time for UnProtect: 0.001 s.
>|
---#TCSETPAR SELECT_CORE BOTH_CORES
>|
---#TPCMD MASSERASE C
Erase already done into Unprotect procedure for both cores.
Time for Masserase C: 0.001 s.
>|
---#TPCMD BLANKCHECK F
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Blankcheck F: 0.096 s.
>|
---#TPCMD PROGRAM F
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Program F: 2.591 s.
>|
---#TPCMD VERIFY F R
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Verify Readout F: 1.197 s.
>|
---#TPCMD VERIFY F S
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Verify Checksum 32bit F: 0.252 s.
>|
---#TCSETPAR SELECT_CORE APPLICATION_CORE
>|
---#TPCMD MASSERASE C
AP[0]: Starting Masserase Chip.
Chip Erased: Erased Flash and UICR Memory for Application core.
Time for Masserase C: 0.174 s.
>|
---#TPCMD BLANKCHECK F
```


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```
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
Time for Blankcheck F: 0.116 s.
>|
---#TPCMD PROGRAM F
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
Time for Program F: 2.516 s.
>|
---#TPCMD VERIFY F R
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
Time for Verify Readout F: 0.956 s.
>|
---#TPCMD VERIFY F S
AP[0]: Start Address: 0x00000000, Size: 0x00100000.
Time for Verify Checksum 32bit F: 0.201 s.
>|
---#TCSETPAR SELECT_CORE NETWORK_CORE
>|
---#TPCMD MASSERASE C
AP[1]: Starting Masserase Chip.
Chip Erased: Erased Flash and UICR Memory for Network core.
Time for Masserase C: 0.175 s.
>|
---#TPCMD BLANKCHECK F
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Blankcheck F: 0.015 s.
>|
---#TPCMD PROGRAM F
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Program F: 0.659 s.
>|
---#TPCMD VERIFY F R
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Verify Readout F: 0.243 s.
>|
---#TPCMD VERIFY F S
AP[1]: Start Address: 0x01000000, Size: 0x00040000.
Time for Verify Checksum 32bit F: 0.055 s.
>|
---#TPCMD DISCONNECT
>|
```

3 – NORDIC nRF5340 example 1MB + 256KB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.109 s
Protect both cores	0.027 s
Unprotect both cores	0.560 s
Blankcheck Flash both cores	0.096 s
Program Flash both cores	2.591 s
Verify Readout Flash both cores	1.197 s
Verify Checksum Flash both cores	0.252 s
Cycle Time	**00:04.891 s**

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4 – NORDIC nRF54L15 example 1524KB Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 25000000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC nRF54L15-xxAA.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE C
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPEND
```

4 – NORDIC nRF54L15 example 1524KB Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[2] IDR: 0x32880000, Type: JTAG connection.
The device access port protection is disabled.
AP[0] ROM table base address 0xE00FE000.
CPUID: 0x411FD210.
Implementer Code: 0x41-[ARM].
Found Cortex M33 revision r1p0.
Program counter value is 0x2000007C.
Cortex M33 core Halted [0.002 s].
Single core device configuration:
 * Device ID: 0x7932C372FE946F80.
 * Part: 0x54B15 - nRF54L15.
 * Variant: 0x41414242 - BBAA - Revision A.
 * Package: 0x5146 - undefined.
 * Ram Size: 0x100 - 256 kByte RAM.
 * Flash Size: 0x5F4 - 1524 kByte FLASH.
Requested Clock is 25.00 MHz.
Generated Clock is 25.00 MHz.
Good samples: 1 [Range 8-8].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 25.00 MHz.
Internal Watchdog Disabled.
Time for Connect: 0.106 s.
>|
---#TPCMD MASSERASE F
Time for Masserase F: 2.146 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.065 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 2.418 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.977 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.281 s.
>|
---#TPCMD DISCONNECT
>|
```


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4 – NORDIC nRF54L15 example 1524KB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.106 s
Masserase Flash (optional)	2.146 s
Blankcheck Flash (optional)	0.065 s
Program Flash	2.418 s
Verify Readout Flash	0.977 s
Verify Checksum Flash	0.281 s
Cycle Time	**00:06.049 s**

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NORDIC NRF Driver Changelog

Info about driver version 1.00 - 20/01/2020
Supported NRF52832 device.

Info about driver version 1.01 - 30/01/2020
Now is possible to read/dump the read only FICR memory.

Info about driver version 2.00 - 05/02/2020
Added support for FlashRunner HS.

Info about driver version 2.01 - 26/02/2020
Improved programming times.

Info about driver version 2.02 - 01/05/2020
Improved programming times.

Info about driver version 3.00 - 21/08/2020
Improved programming times and added new SWD FPGA.

Info about driver version 4.00 - 30/09/2020
Added FPGA for FlashRunner HS and managed Watchdog Software.

Info about driver version 4.01 - 19/10/2020
Supported nRF52833, nRF52832, nRF52810.

Info about driver version 4.02 - 21/10/2020
Supported nRF51822.

Info about driver version 4.03 - 06/11/2020
Supported nRF52840.

Info about driver version 4.04 - 19/11/2020
Improved programming times.

Info about driver version 4.05 - 23/11/2020
Improved programming times.

Info about driver version 4.06 - 26/03/2021
Supported all nRF52xx devices.

Info about driver version 4.07 - 11/06/2021
Supported a lot of Nordic 3rd party modules and modems devices.

Info about driver version 4.08 - 15/06/2021
Supported all Nordic 3rd party modules and modems devices.

Info about driver version 4.09 - 28/06/2021
Added CONNECT_UNDER_RESET option to make an hardware reset before connect procedure.

Info about driver version 4.10 - 19/07/2021
Internal update for FPGA name and version tracking.

Info about driver version 4.11 - 12/08/2021
Upgraded Connect Under Reset Procedure.
Internal upgrade of the algorithm, no change to the operations it performs.

Info about driver version 4.12 - 30/08/2021
Connection procedure updated, now NRF driver automatically find the best entry sequence.

Info about driver version 4.13 - 04/11/2021
Internal update, upgraded management for reset FPGA procedure.

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Info about driver version 4.14 - 25/01/2022
Added READ_MEM8, READ_MEM16, READ_MEM32 commands.

Info about driver version 4.15 - 22/02/2022
Fixed put the device back into normal mode since the overall power consumption is higher in Debug Interface mode.

Info about driver version 4.16 - 14/03/2022
Internal upgrade of the algorithm, no change to the operations it performs.

Info about driver version 4.17 - 16/06/2022
Print current FPGA version loaded into TPSTART command.
Upgraded internal code to align all drivers.

Info about driver version 5.00 - 28/07/2022
Added FPGA for new FlashRunner 2.0 models.

Info about driver version 5.01 - 23/05/2023
Improved Access Port Protect and Unprotect for Single Core device nRF52 series with device revision >= Xxx.
Added Access Port Protect and Unprotect for Dual Core device nRF53 series.

Info about driver version 5.02 and 5.03 - 08-09/06/2023
Supported nrF91 series: supported nRF9160-xxAA.

Info about driver version 5.04 - 04/08/2023
Improved Access Port Protect and Unprotect for Single Core device nRF52 series with device revision >= Xxx.

Info about driver version 5.05 - 23/04/2024
Improved Disconnect procedure when the programming fails to manage correctly Vprog0 and Vprog1 voltages.

Info about driver version 5.06 - 05/11/2024
Supported nrF91 series: supported nRF9131-xxCA, nRF9151-xxCA and nRF9161-xxCA.

Info about driver version 5.07 - 19/11/2024
Supported nrF54L series: supported nRF54L15-xxAA, nRF54L10-xxAA and nRF54L05-xxAA.

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